Notice of Allowability	Application No.	Applicant(s)	
	10/776,016	CHANG, DONG-SOO	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the request for reconsideration dated 5/2/2006*.

2. ☒ The allowed claim(s) is/are *1 and 4-8*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

Claims 1 and 4-8 are allowed.

The following is an examiner's statement of reasons for allowance:

Prior art does not teach or suggest, in combination with the other claimed limitations, that the first impurity region has a higher impurity concentration than the second purity region and the fourth impurity region has impurity concentration *as high as* the third impurity region.

Grider et al., the closest prior art of record, teaches a method similar to the one recited in claim 1, but teaches that the source/drain extensions (ie. the second and fourth impurity regions) are either moderately or lightly doped for *both* the NMOS and PMOS devices, indicating that the first impurity region has higher impurity concentration than the second impurity region *and* the fourth impurity region has higher impurity concentration as the third impurity region (in contrast, claim 1 requires that the fourth impurity region have an impurity concentration as high as, or the same as, the third impurity region).

Wolf (*Silicon Processing for the VLSI Era*, Vol. 3, 1995) teaches that PMOS and NMOS elements on a CMOS device may be processed differently because n-type (in silicon) dopants such as arsenic have heavier ionic masses than p-type dopants such as boron. The result is that during ion implantation, it is more difficult to control the depth of the boron implant than the arsenic implant. Additionally, boron diffuses more readily than arsenic. These factors result in punchthrough and short-channel effects in

the PMOS element. (p. 289, section 5.8.1 and p. 307, section 5.8.3.2). Wolf et al. teaches a variety of techniques known in the art of semiconductor processing to remedy these effects (for example, longer channel lengths, and controlling the depth of the LDD implant by using lower implantation energies—pp. 305-307; see also Ju, U.S. 5,943,565), but does not teach forming a source/drain extension region with an impurity concentration as high as, or the same as, the source/drain impurity concentration. Additionally, as argued by Applicant on 5/02/2006 (p. 3, paragraph 2), Wolf et al. does not teach forming a CMOS device having one element (either NMOS or PMOS) with source/drain regions having impurity concentrations higher than the source/drain extension regions, and the other element (either PMOS or NMOS, respectively) having source/drain extension regions having impurity concentrations as high as, or the same as, the source/drain regions. Wolf and Ju, like Grider et al., teach treating the NMOS and PMOS elements the same regarding the impurity concentrations in the source/drain extension and source/drain regions.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kim et al. (commonly assigned U.S. 2002/0164847) and Yoshino et al. (U.S. 2001/0025994) disclose methods of fabricating a CMOSFET similar to the

method recited in claim 1, but do not teach that the first impurity region has a higher impurity concentration than the second purity region and the fourth impurity region has impurity concentration as high as the third impurity region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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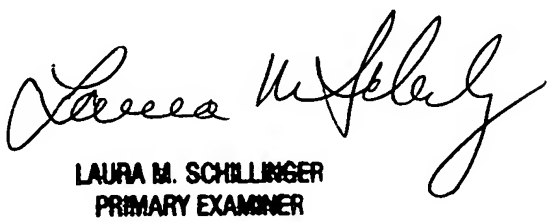

LAURA M. SCHILLINGER
PRIMARY EXAMINER